AL462
Ultra HD FIFO Memory
Application Notes

Version 1.1

Amendments

Revise Date	Contents	Page
03.30.2018	Release version 1.0	/
04.09.2019	Remove P6 to NC, RCKO0/1- always enables Remove section 3.3 - Synchronous output clocks and controls	P.5, P.15 P.14
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Disclaimer

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1. Introduction

The AL462 is a First-In-First-Out (FIFO) memory that consists of 512-Mbits of memory density and can be configured as a 16M x 32-bit and 16M x 16-bit x2 FIFO at maximum R/W operating speed of 150 MHz for HD video applications up to 4K2K Ultra HD resolution. The AL462 Ultra HD (UHD) FIFO can be used in a wide range of applications such as multimedia, video capture systems and many other varieties of video data buffering applications. The size and high-speed data access allow HD video frame capture up to 4Kx2K resolutions.
This document provides information for AL462, including:

- AL462 Key Functions
- AL460A and AL462 Comparison and Design Conversation
- AL462 Electronic Characteristic

2. AL462 Feature

2.1 AL462 Key Feature

The AL462 was designed and manufactured using state-of-the-art technologies with low power consumption AC characteristics (1.8/3.3V power supply) facilitating high performance and high quality applications. The chip is available in LFBGA 249-ball package; the small footprint allows product designers to keep board real estate to a minimum.

- 512-Mbit density, 16Mx32-bit, 16Mx16-bit x2 configuration
- Supports video NTSC, PAL and HDTV up to 4Kx2k resolution
- Independent 32/16-bit read/write operations (different I/O data rates acceptable) at a maximum speed of 150 MHz (-7 version)
- High speed synchronous sequential access
- Input/ Output enable control

2.2 AL462 Block Diagram & Pin Definition

The internal structure of each AL462 consists of Input/ Output buffers, Write Data Registers, Read Data Registers and main 8Mx32-bit, 8Mx16-bit x2 memory cell array and state-of-the-art logic design that takes care of addressing and controlling the read/write data.

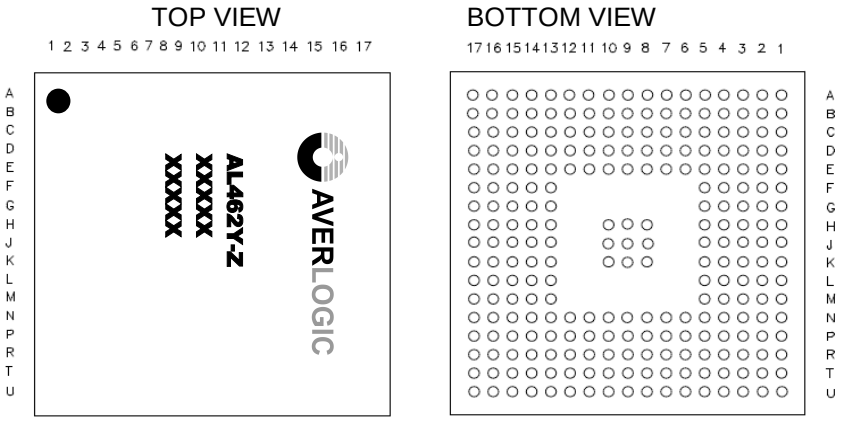


Figure 1. 249 LFBGA Package Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	DI2	DI4	DI6	DI8	DI10	DI12	DI14	VSS33	WCLK0	VSS	NC	VSS	DI18	DI20	DI22	DI24	DI25	A
B	DI1	DI3	DI5	DI7	DI9	DI11	DI13	DI15	VDD33A	VSS33	VDD33C	DI16	DI17	DI19	DI21	DI23	DI26	B
C	DI0	NC	WEN0	WRST0	IE0	DRAM_CFG1	DRAM_CFG3	DRAM_CFG5	DLL_CFG1	NC	NC	NC	NC	TFEN	PLRTY	DI27	DI28	C
D	VSS	VSS33	NC	NC	NC	DRAM_CFG0	DRAM_CFG2	DRAM_CFG4	DLL_CFG0	DLL_CFG2	NC	NC	16EN	NC	WFSEL0	DI29	DI30	D
E	XOUT	VSS	TMOD0	TMOD1	NC	VD33M	VDD	VDD	VDD	VDD	VDD	VSS	DVC18	WFSEL1	WEN1	DI31	VSS33	E
F	XIN	DVC18	NC	TMOD2	NC								DVQ18	NC	WRST1	VDD33B	WCLK1	F
G	VSS	DVC18	DVC18	TEST	NC								VSS	NC	IE1	VSS	VSS33	G
H	NC	NC	NC	NC	NC			AVDD18_PLL1	AVSS_PLL1	DVQ18			VSS	VSS	NC	VDD33D	NC	H
J	FVDD33	FVSS33	VSS	NC	NC			AVDD18_PLL2	AVSS_PLL2	VSS			VSS	VSS	VSS	VSS	VSS	J
K	RSTN	NC	REN0	NC	NC			AVDD18_PLL3	AVSS_PLL3	DVC18			DVQ18	DVQ18	DVQ18	DVQ18	DVQ18	K
L	DO0	RENO0	RRST0	NC	NC								VSS	DVQ18	DVQ18	VSS	VREF2	L
M	DO2	DO1	NC	VSS	NC								VSS33	DVC18	DVQ18	VSS	VSSR1	M
N	DO4	DO3	NC	OE0	VDD33E	VDD	VSS	VSS33	VDD	VDD33G	VSS33	VDD	VSS	VDD	VSS	VSS33	VREF1	N
P	DO6	DO5	NC	NC	RFSEL1	NC	NC	RCKOINV0	NC	NC	RCKOINV1	NC	REN1	RRST1	OE1	VDD33H	VSS33	P
R	DO8	DO7	NC	RFSEL0	NC	NC	NC	NC	NC	NC	NC	NC	RENO1	NC	NC	VDD33F	RCKO1	R
T	DO9	DO11	DO13	DO15	VDD33E	VSS33	VSS	DO16	DO17	DO19	DO21	DO23	DO25	DO27	DO29	DO31	VDD33H	T
U	DO10	DO12	DO14	VSS33	RCLK0	VDD33G	RCKO0	VSS33	DO18	DO20	DO22	DO24	DO26	DO28	DO30	VDD33F	RCLK1	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 2. AL462 249-Ball LFBGA Pin-out Diagram

2.3 Pin Description

Write Bus Signals

Pin Name	Ball No	Type	Description
DI[31:0]	E16, D17, D16, C17, C16, B17, A17, A16, B16, A15, B15, A14, B14, A13, B13, B12, B8, A7, B7, A6, B6, A5,B5, A4, B4, A3, B3, A2, B2, A1, B1, C1	I	32/16-bit data inputs; synchronized with the WCLK clock. Data is acquired at the rising edge of WCLK clock. The mapping between 32-bit and 16-bit x2 bus configuration are; DI[7:0]=DIA[7:0] DI[15:8]=DIA[15:8] DI[23:16]=DIB[7:0] DI[31:24]=DIB[15:8]
WEN0 & WEN1	C3, E15	I	WEN is the write enable signal that controls the 32/16-bit input data write and write pointer operation. WEN0 is write enable signal to control all 32-bit bus operation in 32-bit mode (16EN="L"); WEN0 and WEN1 are write enable signals to control dual 16-bit DIA[15:0] and DIB[15:0] bus operation in 16-bit mode (16EN="H") respectively.
IE0 & IE1	C5, G15	I	IE is the data input enable signal that controls the enabling/ disabling of the 32/16-bit data input pins. The internal write address pointer is always incremented at the rising edge of WCLK by enabling WEN regardless of the IE level. IE0 is data input enable signal to control all 32-bit bus operation in 32-bit mode (16EN="L"); IE0 and IE1 are data input enable signals to control dual 16-bit DIA[15:0] and DIB[15:0] bus operation in 16-bit mode (16EN="H") respectively.
WCLK0 & WCLK1	A9, F17	I	WCLK is the write clock input pin. The write data input is synchronized with this clock. WCLK0 is write clock input to control all 32-bit bus operation in 32-bit mode (16EN="L"); WCLK0 and WCLK1 are write clock inputs to control dual 16-bit DIA[15:0] and DIB[15:0] bus operation in 16-bit mode (16EN="H") respectively.
WRST0 & WRST1	C4, F15	I	The WRST is the write rest signal that resets the write address pointer to 0. WRST0 is write rest signal to control all 32-bit bus operation in 32-bit mode (16EN="L"); WRST0 and WRST1 are write rest signals to control dual 16-bit DIA[15:0] and DIB[15:0] bus operation in 16-bit mode (16EN="H") respectively.
WFSEL0 & WFSEL1	D15, E14	I	Write Frame select pin in Two Frame Mode (TFEN = H): "L": Frame 0 "H": Frame 1 WFSEL0 is write frame select signal to control all 32-bit bus operation in 32-bit mode (16EN="L"); WFSEL0 and WFSEL1 are write frame select signals to control dual 16-bit DIA[15:0] and DIB[15:0] bus operation in 16-bit mode (16EN="H") respectively.

*Note1: For the polarity definition of all write control signals (WEN, IE and WRST), please refer to the PLRTY pin definition and "Memory Operation" section for details.

Read Bus Signals

Pin Name	Ball No	Type	Description
DO[31:0]	T16, U15, T15, U14, T14, U13, T13, U12, T12, U11, T11, U10, T10, U9, T9, T8, T4, U3, T3, U2, T2, U1, T1, R1, R2, P1, P2, N1, N2, M1, M2, L1	O	31/16-bit data outputs; synchronized with the RCLK clock. Data is output at the rising edge of the RCLK clock. The mapping between 32-bit and 16-bit x2 bus configuration are; DO[7:0]=DOA[7:0] DO[15:8]=DOA[15:8] DO[23:16]=DOB[7:0] DO[31:24]=DOB[15:8]
REN0 & REN1	K3, P13	I	REN is the read enable signal that controls the 16-bit output data read and read pointer operation. REN0 is read enable signal to control all 32-bit bus operation in 32-bit mode (16EN="L"); REN0 and REN1 are read enable signals to control dual 16-bit DOA[15:0] and DOB[15:0] bus operation in 16-bit mode (16EN="H") respectively.
OE0 & OE1	N4, P15	I	OE is the data input enable signal that controls the enabling/ disabling of the 16- bit data output pins. The internal read address pointer is always incremented at the rising edge of RCLK by enabling REN regardless of the OE level. OE0 is data output enable signal to control all 32-bit bus operation in 32-bit mode (16EN="L"); OE0 and OE1 are data output enable signals to control dual 16-bit DOA[15:0] and DOB[15:0] bus operation in 16-bit mode (16EN="H") respectively.
RCLK0 & RCLK1	U5, U17	I	RCLK is the read clock input pin. The read data output is synchronized with this clock. RCLK0 is read clock output to control all 32-bit bus operation in 32-bit mode (16EN="L"); OCLK0 and WCLK1 are read clock outputs to control dual 16-bit DOA[15:0] and DOB[15:0] bus operation in 16-bit mode (16EN="H") respectively.
RCKO0 & RCKO1	U7, R17	O	RCLK loop-out clocks
RENO0 & RENO1	L2, R13	O	RENO0 and RENO1 are "read enable" output signals that are synchronous with RCKO0 and RCKO1 output clocks respectively
RCKOINV0 &RCKOINV1	P8, P11	I	RCKO0 & RCKO1 loop-out clock inversion controls; "L": RCKO0 & RCKO1 no inversion. "H": RCKO0 & RCKO1 output inverted
RRST0 & RRST1	L3, P14	I	The RRST is the read reset signal that resets the read address pointer to 0. RRST0 is read rest signal to control all 32-bit bus operation in 32-bit mode (16EN="L"); RRST0 and RRST1 are read rest signals to control dual 16-bit DOA[15:0] and DOB[15:0] bus operation in 16-bit mode (16EN="H") respectively
RFSEL0 & RFSEL1	R4, P5	I	Read Frame select pin in Two Frame Mode (TFEN ="H"): "L": Frame 0 "H": Frame 1 RFSEL0 is read frame select signal to control all 32-

			bit bus operation in 32-bit mode (16EN="L"); RFSEL0 and RFSEL1 are read frame select signals to control dual 16-bit DOA[15:0] and DOB[15:0] bus operation in 16-bit mode (16EN="H") respectively.

**Note2: For the polarity definition of all read control signals (REN, OE, RRST,), please refer to PLRTY pin definition and "Memory Operation" section for details.

*Note3: Signals RCKO, REO and RCKOINV are not available in reversion "A". The active states for the loop-out read clock control signals, REO and RCKOINV are also determined by PLRTY pin definitions: active "High" when PLRTY is "GND", active "Low" when PLRTY is "VDD".

Power/Ground Signals

Pin Name	Ball No	Type	Description
DVC18, DVQ18	F2, G3, G2, M14, M15, L14, L15, K13, K14, K10, K15,K16, H10, K17, F13, E13	PW	1.8V ±5% power supply for internal memory
VDD	E7,N6,N14,N9,N12,E11,E9,E10,E8	PW	1.8V ± 5% power supply for internal control logic
AVDD18_PLL1,AVDD18_PLL2,AVDD18_PLL3	H8, J8, K8	PW	1.8V ±5% power supply for PLL
VDD33A, VDD33B, VDD33C, VDD33D	B9, F16, B11, H16	PW	3.3V ± 5% power supply for input I/O
VDD33E,VDD33F,VDD33G,VDD33H	N5, T5, U16, R16, U6, N10, T17, P16	PW	3.3V ± 5% power supply for output I/O
FVDD33	J1	PW	3.3V ± 5% power supply for internal logic
VD33M	E6	PW	3.3V ± 5% power supply for internal logic
VSS	D1,E2,G1,J3N7,N15,T7, N13,M4,M16,L13,L16, H13,J14,J15,J13,J16,J10,H14,G13,E12,J17,A12,G16,A10	GND	Internal memory chip GND
VSS33	D2,M13,U4,T6, N16,N8,U8,N11,P17, G17,B10,E17,A8	GND	Input/ Output data I/O GND
FVSS33	J2	GND	GND
AVSS_PLL1,AVSS_PLL2,AVSS_PLL3	H9, J9, K9	GND	PLL GND

Miscellaneous Signals

Pin Name	Ball No	Type	Description
RSTN	K1	I	Global reset (active Low)
PLRTY	C15	I	Select active polarity of the control signals including WEN, REN, WRST, RRST, IE, OE, ROEN and ROINV (total of 8 signals) PLRTY = VDD33, active low. PLRTY = GND, active high. Note: during memory operation, the pin must be permanently connected to VD33 or GND. If PLRTY level is changed during memory operation, memory data is not guaranteed.
XIN	F1	I	Crystal/oscillator input 27 MHz

			* Minimum crystal frequency accuracy: ±100 ppm TMOD2 pin pull-down to enable XIN pin
XOUT	E1	O	Crystal output
VREF1	N17	AI	Reference voltage input * Please refer to “External decoupling circuit” application note for details
VREF2	L17	AI	Reference voltage input 2 * Please refer to “External decoupling circuit” application note for details
VSSR1	M17	-	Reference voltage ground * Please refer to “External decoupling circuit” application note for details
16EN	D13	I	16-bit bus configuration enable “L” – 32-bit Input and Output bus width (Default) “H” – 16-bit x2 Input and Output bus width
TFEN	C14	I	Two frame mode enable: “L” – Standard FIFO Mode “H” – Two Frame Mode
TEST	G4	I	Test pin (pull-down for normal operation, internal floating)
TMOD0	E3	I	Pull 10K ohm to “H” (“H” for normal operation, internal floating)
TMOD1	E4	I	Pull 10K ohm to “H” (“H” for normal operation, internal floating)
TMOD2	F4	I	“H” for OSC input, “L” for XTAL input (internal floating)
DLL_CFG[2:0]	D10, C9, D9	I	Pull 10K ohm to “H” (“H” for normal operation)
DRAM_CFG[5:0]	C8,D8,C7,D7,C6,D6	I	Pull 10K ohm to “H” (“H” for normal operation)
NC	A11,C2,C12,C13,D3,D4,D5,D11,D12,D14,E5,F3,F5,F14,G5,G14,H1,H2,H3,H4,H5,H15,H17,J5,K2,M3,N3,P3,P4,P6,P7,P9,P10,P12,R3,R5,R6,R7,R8,R9,R10,R11,R12,R14,R15,J4,K4,,K5,L4,L5,M5,C10,C11,D11	-	No connect

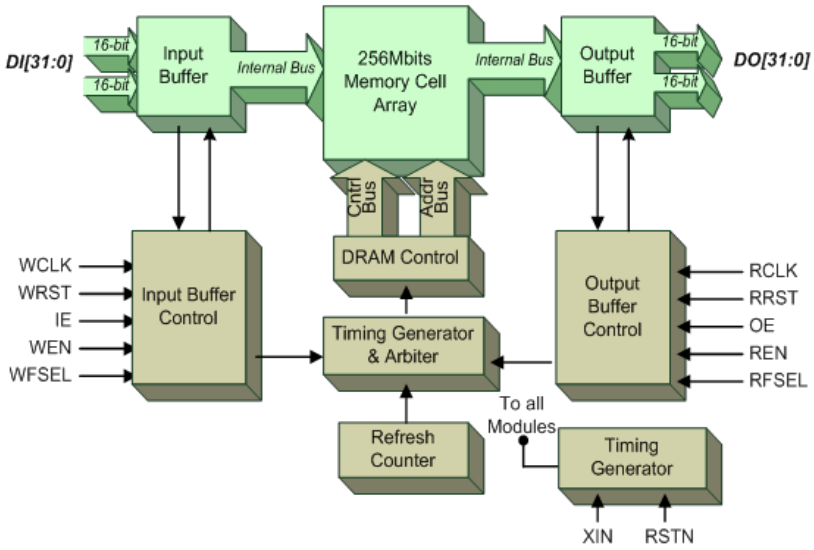
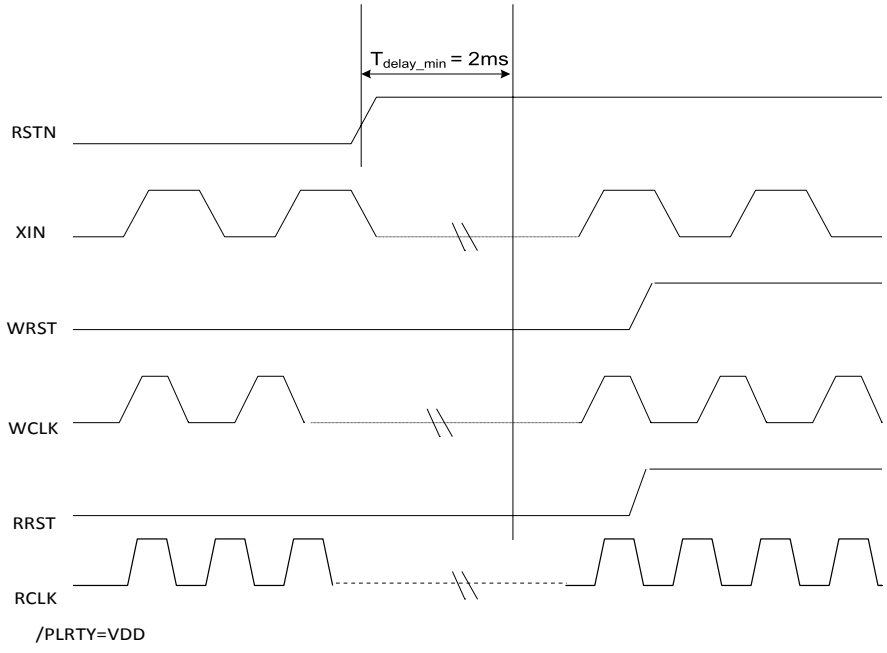


Figure 3. Chip Function Block Diagram

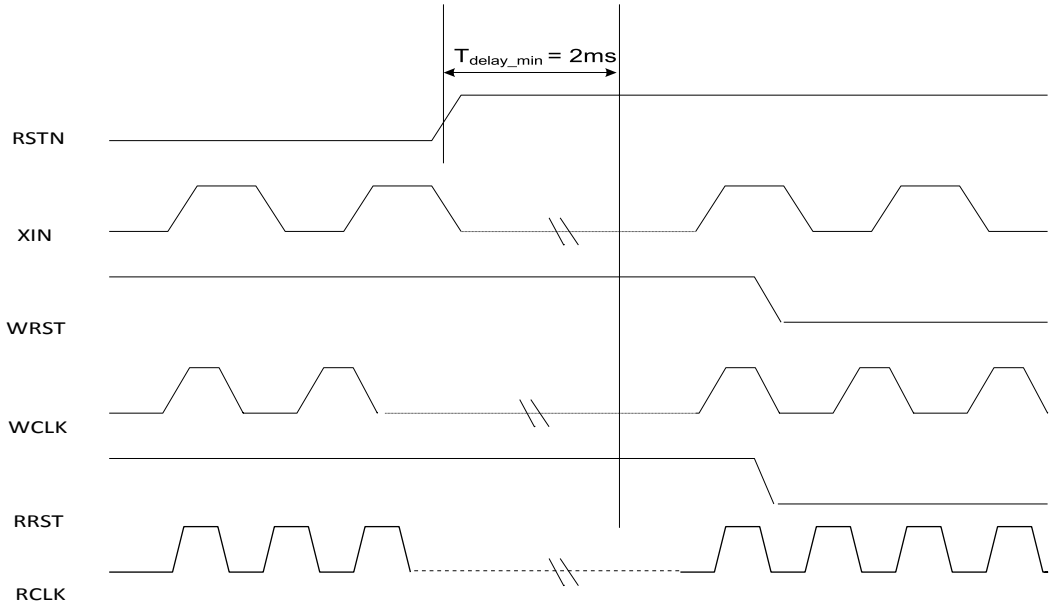
3. AL462 Design Consideration

3.1 Power-on Global Reset and Initialization for AL462B

During system power up, a power-on-reset is required for successful initialization of FIFO internal logic. After deactivation of its reset state, wait for T_{delay_min} (2 ms) before applying any operations to ensure the FIFO is in the normal operating state. Apply a valid reset pulse of WRST and RRST after power-on-reset to guarantee Read/Write operations start at a known address (address point at zero). The following diagrams
illustrate global reset and R/W reset timings at power-up with polarity equals VDD and GND



Chip Reset& R/W Reset Timing (Power-on-reset)



/PLRTY=GND

Chip Reset& R/W Reset Timing (Power-on-reset)

Following is a reference RC circuit.

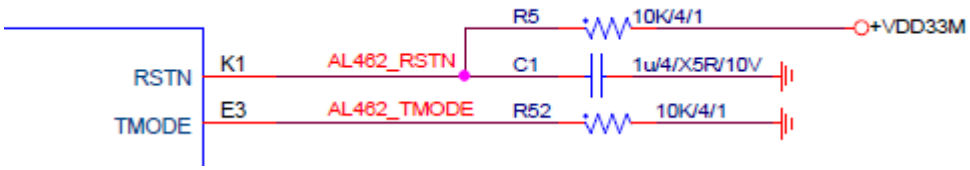


Figure 6. Reset Circuit for RSTN

3.2 AL462 16-bit mode simultaneous operation

AL462 is designed to support single 32-bit bus and dual 16-bit bus configurations. The selection of 32-bit or 16-bit x2 mode is controlled by the signal “16EN” pin. The corresponding control pins for 32-bit and 16-bit are illustrated in the table.

Single 32-bit Mode (16EN= Ground/Low)

Data Pin	Control Pins	Description
DI[31:0]	WEN0, IE0, WCLK0, WRST0, WFSEL0	32-bit data inputs & controls; 32-bit data are synchronized with the WCLK0 clock. Data are acquired at the rising edge of WCLK0 clock. The operating polarity of control signals are defined by the state of the PLRTY pin.

DO[31:0]	REN0, OE0, RCLK0, RRST0, RFSEL0	32-bit data outputs & controls; 32-bit are synchronized with the RCLK0 clock. Data are output at the rising edge of the RCLK0 clock. The operating polarity of control signals are defined by the state of the PLRTY pin.

Table 1. 32-bit Mode I/O and Control Pin Assignment

Dual 16-bit Mode (16EN = VDD/High)

Data Pin	Control Pins	Description
DI[15:0]	WEN0, IE0, WCLK0, WRST0, WFSEL0	16-bit data inputs & controls; 16-bit data are synchronized with the WCLK0 clock. Data are acquired at the rising edge of WCLK0 clock. The operating polarity of control signals are defined by the state of the PLRTY pin.
DO[15:0]	REN0, OE0, RCLK0, RRST0, RFSEL0	16-bit data outputs & controls; 16-bit data are synchronized with the RCLK0 clock. Data are output at the rising edge of the RCLK0 clock. The operating polarity of control signals are defined by the state of the PLRTY pin.
DI[31:16]	WEN1, IE1, WCLK1, WRST1, WFSEL1	16-bit data inputs & controls; 16-bit data are synchronized with the WCLK1 clock. Data are acquired at the rising edge of WCLK0 clock. The operating polarity of control signals are defined by the state of the PLRTY pin.
DO[31:16]	REN1, OE1, RCLK1, RRST1, RFSEL1	31-bit data outputs & controls; 16-bit data are synchronized with the RCLK1 clock. Data are output at the rising edge of the RCLK1 clock. The operating polarity of control signals are defined by the state of the PLRTY pin.

Table 2. 16-bit Mode I/O and Control Pin Assignment

4. AL440B, AL460A & AL462 Design Conversion

4.1 AL440B, AL460A and AL462 Feature Mapping

The AL440B and AL460A FIFO can be replaced by AL462B which provides higher memory density with two bus width configuration as wide as 32-bit. Their feature mappings are shown in the Table below:

Features	AL440B	AL460A FHD FIFO	AL462B UHD FIFO
Memory Size	4Mbit	128Mbit	512Mbit
Bus Width	8-bit	16-bit	32-bit or 16-bit
Configuration	512Kx8	8M×16	Single 16Mx32 or Dual 16Mx16
Max Clock Speed	80MHz & 40MHz	150MHz & 75MHz	150MHz & 75MHz
Clock Mode	Single	Single	Single
Access Mode	Synchronous	Synchronous	Synchronous
Write Control	WE, WRST	WE, WRST	WE0, WRST0 & WE1, WRST1
Read Control	RE, RRST	RE, RRST	RE0, RRST0 & RE1, RRST1
Input Enable	IE	IE	IE0 & IE1
Output Tri-state	OE	OE	OE0 & OE1
Signal Polarity	Selectable	Selectable	Selectable
Core Voltage	3.3V	2.5V	1.8V
I/O voltage	3.3V	3.3V	3.3V or 1.8V
2-Frame Mode	*None*	4M×16×2	4Mx32x2 or Dual 2Mx16x2
Package	44-pin TSOP(II)	128-LQFP	249-LFBGA
Temperature	0 – 70 degree C	0 – 70 degree C	0 – 70 degree C

Table 3. AL440B, AL460A and AL462 Feature Comparison Table

4.2 AL460A to AL462 Conversion

1. Power Consideration

Both AL460A and AL462 are mixed power designs. The supply voltages of AL460A are 2.5V and 3.3V for core and I/O powers respectively. The supply voltage of AL462's core power is 1.8V, while its I/O can be supplied with either 1.8V or 3.3V, depending on the application.

2. Clock Supply for Xin and Xout

Both AL460A and AL462 require main clock input to XIN for chip operation. AL460A can accept either 11.059Mhz, 20.000Mhz, 24.576 MHz or 14.318Mhz clock frequencies, whereas

AL462 only accepts a frequency of 27MHz. The reference circuit design of crystal input for Xin and Xout pins is illustrated in Figure 8.

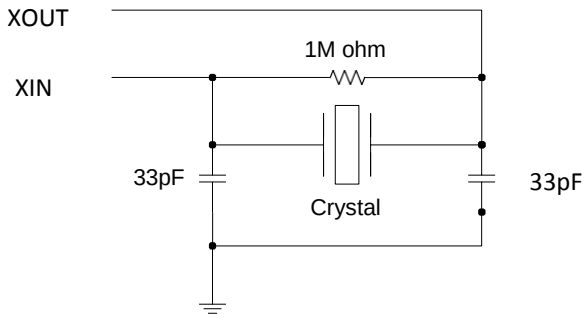


Figure 8. Xin and Xout Reference Circuit

Note: The component values in the circuit are for reference only and could be varying upon Crystal vendors.

3. Power-on Global Reset

Power-up initialization is required for both AL460 and AL462.

5. Data Bus and Controls

AL462 supports single 32-bit bus and dual 16-bit bus modes. The 16-bit bus AL460 design can be replaced with AL462 setting as single 32-bit mode or dual 16-bit mode. The detailed setup of single 32-bit bus mode and dual 16-bit bus mode, their pin mappings are described in datasheet.

6. Synchronous Output Clocks and Controls

The AL462B supports gated clocks RCKO0/RCKO1 and read control RENO0/RENO1 outputs as an alternative for data read operations. The data reading device, such as FPGA, can enable output read clock RCKO and output read enable RENO. The output data DO[31:0] have better synchronous timing with gated clock RCKO0 and RENO0. In 16bit x2 mode, RCKO0/RENO0 and RCKO0/RENO1 can also be used for reading DO[31:24] and DO[23:0] data respectively. The detailed pin definitions of output clocks and controls are specified in the “Pin Description” section.

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